ABSTRACT OF THE DISCLOSURE

A system is provided for testing a physical layer device, or various network portions connected to that physical layer device. The test system includes a random bit generator that, during use, produces a random pattern of bits clocked in parallel onto the transmit portion of the physical device. The parallel-fed information can then be serialized and selectably fed back to the receive input of the same physical device. The receive portion of the physical device can then deserialize the random pattern of bits, and present those bits to logic within the test system. The test system can, therefore, compare each of the random pattern of bits presented to the physical device with corresponding bits derived from the deserializer. If each bit within the random pattern of *m* bits forwarded to the serializer does not compare with each corresponding *m* bits forwarded from the deserializer, then the physical device is known to be a failure. Instructions which begin and end the test operation are forwarded from a test device that is linked to the test system by a JTAG access port configured according to IEEE Std. 1149.1. This allows non-proprietary instructions to be sent into the access port controller, using only a single input pin among the four-pin JTAG access port, where a decoder within the test system is programmed to decode that instruction and either begin or end the test operation. A clock generation circuit will generate a high speed clock, for use by the physical device, to allow the physical device to operate at speed without requiring a costly test system to generate a high-speed clock and signals proprietary to that test system.